

ABSTRACT

Methods are described for fabricating semiconductor devices and transistors thereof, in which a patterned gate length is measured and offset spacers are formed along the sides of the patterned gate prior to drain extension implants, wherein the offset spacer width is controlled according to the measured gate length. This facilitates consistent control over transistor channel length despite variability in the patterned gate length dimension from wafer to wafer and/or from lot to lot.

10